AF

PATENT 1763

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/611,037
Applicant:	:	Kuthi, et al.
Filed:	:	July 6, 2000
Title:	:	METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE
TC/A.U.	:	1763
Examiner	:	Alejandro Mulero, L.
Atty. Docket No.	:	LAM1P077A
Date:	:	March 3, 2005

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on **March 3, 2005**.

Signed: _____
Elizabeth Krcik

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION -- 37 CFR 192)

Commissioner for Patents
Mail Stop: Appeal Brief- Patents
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is in furtherance of the Notice of Appeal filed in this case on November 29, 2004. The Notice of Appeal was received by the USPTO on December 3, 2004. A 1-month extension of time is requested herein, extending the deadline for filing this Appeal Brief to March 3, 2005.

This application is on behalf of:

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity) ☒ $500.00 (Large Entity)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

Attorney Docket No.: LAM1P077A

☒ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Months	Large Entity	Small Entity
☒ one	$120.00	$60.00
☐ two	$450.00	$225.00
☐ three	$1,020.00	$510.00

☒ If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for __ months has already been secured and the fee paid therefor of $_____is deducted from the total fee due for the total months of extension now requested.

☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Total Fees Due:

Notice of Appeal Fee	$500.00
Extension Fee (if any)	$120.00
Total Fee Due	**$620.00**

☒ Enclosed is Check No. 13630 in the amount of $620.00.

☒ Charge any additional fees or credit any overpayment to Deposit Account No. 50-0850, (Order No. LAM1P077A).

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Rick von Wohld, Esq.
Registration No. 48,018

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
(408) 749-6900
Customer No. 25,920

Attorney Docket No.: LAM1P077A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE KUTHI, ET AL.

Application for Patent

Filed July 6, 2000

Application No. 09/611,037

FOR:

METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE

APPEAL BRIEF

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450, on April 23, 2004.

Signed: _____
Elisabeth Krcik

MARTINE PENILLA & GENCARELLA, LLP
Attorneys for Applicants

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I. REAL PARTY IN INTEREST

The real party in interest is Lam Research Corporation, the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of any related appeals and/or interferences.

III. STATUS OF THE CLAIMS

A total of 40 claims were presented during the prosecution of the present application. Applicants canceled claims 1-13 and 22-32. Applicant appeals the final rejection of claims 14-21 and 33-40.

IV. STATUS OF THE AMENDMENTS

No Amendment has been filed subsequent to Final Rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

In one embodiment of the invention, Applicants claim a method for processing a semiconductor wafer through plasma etching operations. The method is claimed in a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode (see Applicants' specification as filed, page 6, lines 8-12, Figure 1A). The method includes striking a plasma in a plasma region of the chamber, and generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer, and a decrease in bias voltage directed at the top electrode (page 16, line 19 - page 17, line 7, Figure 4A). The top electrode includes a center region, a first surface and a second surface. The first surface includes an inlet that is configured to receive processing gases from a source that is external to the chamber, and to flow the processing gases into the center region. The second surface includes a plurality of gas feed holes (228, Figs. 2A, 2E) that lead to a plurality of electrode openings (202b, Figs. 2A, 2B, 2C, 2D, 2E) that have electrode opening diameters (242, Figs. 2C, 2D) that are greater than gas feed hole diameters (240, Figs. 2C, 2D) of the plurality of gas feed holes (228). The plurality of electrode openings (202b) are configured to define the second surface which is located over the wafer surface (236, Fig. 2E) of the semiconductor

wafer. According to the method, when a plasma is struck in the plasma region (212, Fig. 2E) defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface (232, Fig. 2E) having a first plasma sheath surface area that is proximate to the wafer surface, and a second plasma sheath surface (231, Fig. 2E) having a second plasma sheath surface area that is proximate to the second surface. The second plasma sheath surface area is greater than the first plasma sheath surface area (Figs. 2E, 3, and page 14, line 11 - page 15, line 6, Table A).

In another embodiment, Applicants claim a method of processing a semiconductor wafer. The method includes providing a processing chamber. The processing chamber is in an operational state and includes a top electrode, a wafer support chuck having the semiconductor wafer positioned thereon, and a pair of RF power sources (see Applicants' specification as filed, page 6, lines 8-12, page 13, lines 19-22, Figure 1A). The method further includes striking a plasma within a plasma region (212, Fig. 2E) of the processing chamber, and causing a first surface of a plasma sheath (231, Fig. 2E) to shift (Figs. 2E, 3, 4A) into electrode openings (202b, Figs. 2A, 2B, 2C, 2D, 2E) of the top electrode. The plasma sheath defines the first surface of the plasma sheath (231, Fig. 2E) next to the top electrode (200, Fig. 2A) and a second surface (232, Fig. 2E) of the plasma sheath over a surface of the semiconductor wafer (206, Fig. 2E).

In a further embodiment, Applicants claim a method for high aspect ratio semiconductor etching (page 17, lines 16-21). The method includes providing a plasma etch processing chamber. The plasma etch processing chamber includes a top electrode, a wafer support chuck, and a pair of RF power supplies (see Applicants' specification as filed, page 6, lines 8-12, Figure 1A). The plasma etch processing chamber is configured to be in an operational state (page 13, lines 19-22). The method further includes striking a plasma in a plasma region (212, Fig. 2E) of the plasma etch processing chamber. The plasma region is defined between an electrode surface of the top electrode (200, Fig. 2A), and a wafer surface of a wafer positioned on the wafer support chuck (206, 236, Fig. 2E). The method then includes causing a first surface (231 Figs. 2E, 3) of a plasma sheath to shift into electrode openings of the top electrode (202b, Fig. 2E). The first surface of the plasma sheath is proximate to the top electrode. The method provides for increasing a bias voltage over the wafer

surface while decreasing the bias voltage over the electrode surface of the top electrode without increasing a plasma density (Page 17, lines 1-23, Figs. 4A, 4B, 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds for rejection to reviewed on appeal are as follows:

Claims 37-40 were finally rejected under 35 USC §112, second paragraph;

Claims 33-35, 37-38, and 40 were finally rejected under 35 USC §103(a); and

Claims 14-21, 36, and 39 were finally rejected under 35 USC §103(a).

VII. ARGUMENT

A. Claims 37-40 are not indefinite, and are therefore not properly rejected under 35 USC §112, second paragraph.

Claims 37-40 stand rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Specifically, the Office has deemed the term "high aspect ratio" as being a relative term rendering the claims indefinite.

"High aspect ratio" is best characterized as a term of art that is well known and understood by one of ordinary skill in the art. Exemplary of the common usage and understanding of the term is the patent to Tomita et al. (U.S. Patent No. 5,593,540), cited by Examiner. In Tomita et al., the term high aspect ratio is used in the Background of the Invention section at col. 1, lines 36-38, "An anisotropic etching having a high aspect ratio is utilized for the manufacture of a semiconductor device having a finer pattern." Compare this to Applicants' use of high aspect ratio in the Background of the Invention of the instant application: "As the demand to etch smaller and smaller integrated circuit device patterns continues to increase, more difficult high aspect ratio etching will be needed" (page 3, lines 22-23). Applicants further describe high aspect ratio in relation to etch geometry at page 4, lines 4-6: "As the aspect ratios continue to increase (*i.e.*, deeper and narrower etching geometries), a process window that defines a set of controllable process parameters will also rapidly shrink." And, according to Tomita et al., "For achieving an anisotropic etching with a high aspect ratio, it is necessary to set the inner pressure of

the process chamber at a low level, leading to a plasma polymerization of the treating gas" (col. 1, lines 38-41).

Tomita et al. further describe, and illustrate, high aspect ratio at col. 5, lines 60-64: "FIG. 8 is a cross sectional view showing a wafer etched with a high aspect ratio. It is seen that the wafer is etched uniformly both in the central portion and in the peripheral portion."

In rejecting claims 37-40 for indefiniteness, the Examiner has asserted that, "Clearly, what constitutes a 'high aspect ratio' has changed over the years with the further development of semiconductor technology and the meaning of this term may not be the same to different people having ordinary skill in the art. For this reason, the rejection is maintained." It is true that the present application is a continuation of an application filed on June 16, 1998, and the technology has certainly advanced since the date of filing, but in accordance with MPEP §2173.02, "Definiteness of claim language must be analyzed, not in a vacuum, but in light of: (A) The content of the particular application disclosure; (B) The teachings of the prior art; and (C) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art ***at the time the invention was made***" (emphasis supplied). Further, "The meaning of every term used in a claim should be apparent from the prior art or from the specification and drawings ***at the time the application is filed***" (MPEP §2173.05(a), emphasis supplied). Applicants respectfully submit that the term "high aspect ratio" is used in a manner consistent with the usual and customary manner throughout the application as filed as would be used by one of ordinary skill in the art at the time of invention, that known prior art, including the prior art used as reference prior art in the prosecution of the instant application, uses the same term in an essentially similar manner, and that one of ordinary skill in the art at the time of invention is clearly and effectively provided the requisite degree and scope of the present invention.

Applicants therefore respectfully submit that claims 37-40 are definite and patentable under 35 USC §112, second paragraph, and that the rejection of these claims is improper and should be withdrawn.

B. Claims 33-35, 37-38, and 40 are not rendered obvious by the patent to Tomita et al. in view of admitted prior art.

Claims 33-35, 37-38, and 40 stand rejected under 35 USC §103(a) as being unpatentable over Tomita et al. (U.S. Patent No. 5,593,540) in view of admitted prior art.

Tomita et al. disclose a plasma etching system including a process chamber for enclosing a plasma, and a means for evacuation of the plasma from the chamber. A substrate is supported on a chuck electrode, and a shower electrode is positioned facing the chuck electrode. The shower electrode has a plurality of small holes. A power source is provided to strike a plasma between the chuck electrode and the shower electrode. Plasma forming gases are supplied through the small holes into the space between the chuck electrode and the shower electrode. The gas is supplied through the small holes at a mass flow rate of at least 620 $kg/m^2/hr$.

Applicants' independent claim 33 claims a method of processing a semiconductor wafer. The method includes providing a processing chamber. The processing chamber is in an operational state and includes a top electrode, a wafer support chuck that has the semiconductor wafer positioned thereon, and a pair of RF power sources. The method then includes striking a plasma within a plasma region of the processing chamber, and causing a first surface of a plasma sheath to shift into electrode openings of the top electrode. The plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

Applicants' independent claim 37 claims a method for high aspect ratio semiconductor etching. The method includes providing a plasma etch processing chamber which includes a top electrode, a wafer support chuck, and a pair of RF power supplies, and is configured in an operational state. A plasma is struck in a plasma region of the chamber. The plasma region is defined between an electrode surface of the top electrode and a wafer surface of a wafer which is positioned on the wafer support chuck. A first surface of a plasma sheath which is proximate to the top electrode is caused to shift into electrode openings of the top electrode. A bias voltage over the wafer surface is increased while the bias voltage over the electrode surface of the top electrode is decreased without increasing a plasma density.

In rejecting claims 33-35, 37-38, and 40, the Examiner has asserted that, "Note that inherently the plasma sheath will form within the inlet opening 55 to form the

second plasma sheath surface area since the openings have an opening diameter of 0.6 mm (see Applicants' specification at page 13, lines 22-24 and col. 5-line 3-5 of Tomita et al.)" The cited section in Applicants' specification as filed recites the following:

> Because the electrode openings 202b have been increased to be at least equal to or greater than about 0.5 mm, a plasma sheath 231 is caused to shift into the electrode openings 202b.

The reference citation to Tomita et al. discloses small holes having a diameter of 0.6 mm. A feature or characteristic common to the presently claimed invention and the Tomita et al. reference does not support an assertion of ***inherency***. The size of the electrode openings is but one parameter or feature of the presently claimed method. It is not a valid assumption to conclude that any electrode having electrode openings of a particular size (in the instant application the size is recited to be at least 0.5mm) will result in a plasma shift into the electrode openings.

Inherency is not supported by the size of the holes in the electrode alone. According to MPEP §2112, "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." The essential premise and basic design taught by Tomita et al. is to ***prevent or avoid*** what the Examiner has asserted is inherent. A side by side comparison of the electrode features described, illustrated, and claimed by Applicants, and the design of the electrode of the Tomita et al. reference clearly illustrate that what the Examiner has maintained is without support in mechanical design and plasma physics:

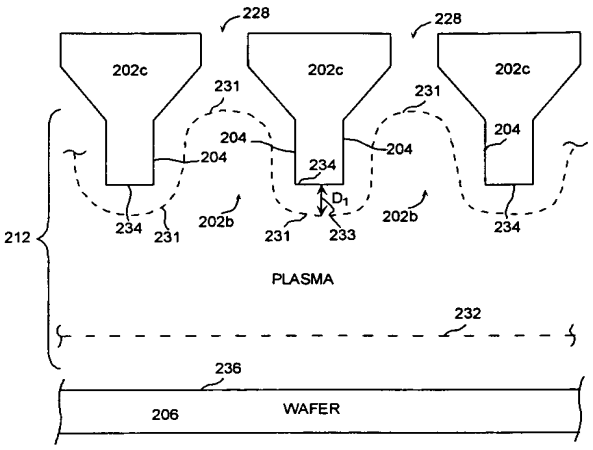


FIG. 2E

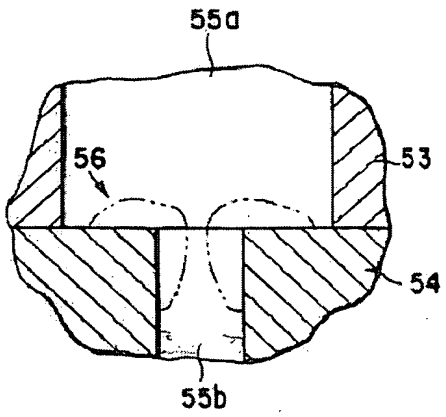


FIG. 4

The figure (Fig. 2E) on the left shows the electrode design claimed by Applicants. The figure on the right is Fig. 4 from the Tomita et al. reference. Applicants claim, for example, "causing a first surface of a plasma sheath to shift into electrode openings of the top electrode," (claim 33) and "causing a first surface of a plasma sheath to shift into electrode openings of the top electrode, the first surface of the plasma sheath being proximate to the top electrode," (claim 37). Among other design features, the gas feed holes (228) are smaller than the electrode openings (202b), which allows the shift to occur while preventing plasma formation in the gas feed holes (228). Contrast that to, among other features such as gas flow, plasma density, etc, the gas feed holes (55a) of the Tomita et al. electrode being ***larger*** than the electrode openings (55b). The fact that the electrode openings (55b) of Tomita et al. may be 0.6 mm, does not support that plasma formed adjacent to that electrode will inherently shift into the electrode openings as claimed by Applicants.

Applicants have submitted a Declaration further supporting that one of ordinary skill in the art would not accept that the size of the electrode opening alone would result in a shift of the plasma sheath. As recited in the MPEP at §2112, "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.'" Further, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." The

Tomita et al. apparatus is constructed in such a manner as to prevent plasma flow into the electrode openings, and Tomita et al. teach away from such plasma flow. Such plasma flow is ***undesirable*** in an apparatus as disclosed by Tomita et al.

In the Declaration Applicants have submitted in the instant application, Inventor Lumin Li asserts the following at paragraph 8:

The objective of the reference patent is preventing polymer deposition. The size of the holes in the showerhead must be small enough to obtain the certain disclosed flow speed. At the same time, the flow speed must be maintained to prevent plasma light up inside the holes. A diameter of 0.6mm does not inherently shift the plasma sheath into the openings and create a surface area next to the electrode that is larger than the surface area that is next to the wafer. It is against common sense, basic plasma physics, and design rules for those skilled in the art -- that is, one of average competence and expertise in the field of plasma etch, would not modify the reference in such a manner as to increase size of the holes and purposely create plasma inside holes.

For at least the above reasons, Applicants submit that independent claims 33 and 37 are patentable over Tomita et al. in view of admitted prior art under 35 USC §103(a). Dependent claims 34-35, 38, and 40, each of which depends directly or indirectly from one of independent claims 33 and 37 are patentable for at least the same reasons. Applicants therefore submit that the rejection of claims 33-35, 37-38, and 40 under 35 USC §103(a) as being unpatentable over Tomita et al. in view of admitted prior art is improper and should be withdrawn.

C. Claims 14-21, 36, and 39 are not rendered obvious by the patent to Tomita et al. in view of admitted prior art, and further in view of the patent to Chang et al.

Claims 14-21, 36, and 39 stand rejected under 35 USC §103(a) as being unpatentable over Tomita et al. in view of admitted prior art as applied to claim 33-35, 37-38, and 40 above, and further in view of Chang et al. (U.S. Patent No. 4,854,263).

The rejection of claims 14-21, 36, and 39 is asserted on the foundation of the rejection of claims 33-35, 37-38, and 40. The arguments presented above in section B are therefore applicable to the present rejection, and are re-submitted in their entirety.

In finally rejecting claims 14-21, 36, and 39, the Examiner asserts that the Tomita et al. reference fails to expressly disclose where the electrode opening diameters are greater than the gas hole feed diameters. Applicants submit that Tomita et al. illustrate in Figure 4 (see above), and describe in the associated text (see col. 5, lines 14-20) that a small hole 55b formed in the cathode plate 54 is smaller than a small hole 55a formed in the cooling plate 53. If the Tomita et al. structure were to be modified in accordance with the electrode and gas feed openings as taught by Chang et al., the principle of operation of the Tomita et al. apparatus would be changed in such a manner as to render the Tomita et al. apparatus ineffective or inoperable for its intended purpose. In accordance with MPEP §2143, such a change in the principle of operation is insufficient to render the claims *prima facie* obvious.

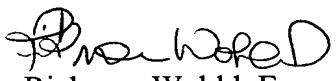
Tomita et al. disclose an apparatus and structure to ***prevent*** plasma from flowing into the small holes 55b. As stated at col. 2, lines 46-52, "The particular gas supply system employed in the present invention permits suppressing the plasma polymerization within the small holes, with the result that a polymer is unlikely to be deposited on the circumferential wall of the small hole. Even if a polymer is formed, the polymer is blown away by the gas stream flowing at a high speed." If the asserted combination would allow plasma flow into the small holes, then the polymerization formation sought to be prevented and overcome would be re-introduced. Similarly, in a re-formed electrode and gas feed hole structure as proposed, a primary principle of operation of the Tomita et al. structure is not only modified, but defeated. Although the Examiner asserts that such a combination would be obvious to enhance dissociation and reactivity of the gases, the Examiner is mistaken. To modify the apparatus in such a manner would not only modify the principle of operation of the apparatus, but it would defeat the principle of operation.

As stated in the attached Declaration at paragraph 2, "The reference patent teaches how to prevent polymer deposition in the small holes of a showerhead electrode by high speed of gas flow. To achieve a mass flow speed of at least 620 $kg/m^2/hr$, the reference specifies the diameter of the holes in the showerhead must be smaller than 0.6 mm. The reference specifies 0.6 mm as the maximum diameter of the hole. Any hole larger than 0.6 mm will reduce gas speed and cannot prevent polymer deposition." The proposed modification of the Tomita et al. electrode would essentially result in the polar opposite of the structure as illustrated in Fig. 4 of the reference (see above), *i.e.*, a gas feed hole that is *smaller* than the electrode opening.

In order to achieve and maintain the high speed gas flow taught by Tomita et al., the disclosed and illustrated structure must be maintained. Tomita et al. address gas dissociation and reactivity by use of buffer plates (as pointed out by the Examiner) and baffle plate 50. The asserted modification could not achieve and maintain the high speed gas flow, and therefore the asserted modification and combination would render the prior art unsatisfactory for its intended purpose.

The asserted combination fails to teach all the claim limitations, and fails to establish a requisite motivation for combination since the combination would change the principle of operation of the Tomita et al. apparatus. Applicants therefore submit that independent claims 14, 33, and 37 are patentable under 35 USC §103(a) over Tomita et al. in view of admitted prior art and further in view of Chang et al. for at least the above reasons. Dependent claims 15-21, 36, and 39, each of which depends directly or indirectly from one of independent claims 14, 33, and 37 are likewise patentable for at least the same reasons. Applicants therefore submit that the rejection of claims 14-21, 36, and 39 under 35 USC §103(a) as being unpatentable over Tomita et al. in view of admitted prior art as applied to claim 33-35, 37-38, and 40 above, and further in view of Chang et al. is improper and should be withdrawn.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP



Rick von Wohld, Esq.
Reg. No. 48,018

MARTINE PENILLA & GENCARELLA, LLP
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
Customer Number 25920

APPENDIX A

CLAIMS ON APPEAL

14. In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode, a method for processing a semiconductor wafer through plasma etching operations, comprising:

striking a plasma in a plasma region of the chamber; and

generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer and a decrease in bias voltage directed at the top electrode, the top electrode having a center region, a first surface and a second surface, the first surface having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface which is located over the wafer surface of the semiconductor wafer,

wherein when a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath surface having a second plasma sheath surface area that is proximate to the second surface, the second plasma sheath surface area being greater than the first plasma sheath surface area.

15. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

causing the second plasma sheath surface having the second plasma sheath surface area to shift into the electrode openings of the second surface of the top electrode, the electrode openings being at least 0.5 mm or greater in diameter and the gas feed holes having a diameter of about 0.1 mm.

17. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the second surface and the wafer surface.

19. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at between about 0.5 mm and about 5 mm.

21. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath surface area is greater than the first plasma sheath surface area.

33. A method of processing a semiconductor wafer, comprising:

providing a processing chamber, the processing chamber being in an operational state and including a top electrode, a wafer support chuck having the semiconductor wafer positioned thereon, and a pair of RF power sources;

striking a plasma within a plasma region of the processing chamber; and

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode,

wherein the plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

34. The method of processing a semiconductor wafer as recited in claim 33, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of the second surface of the plasma sheath.

35. The method of processing a semiconductor wafer as recited in claim 33, further comprising increasing a bias voltage over the surface of the semiconductor wafer while slightly decreasing the bias voltage over a surface of the top electrode and without increasing a plasma density.

36. The method of processing a semiconductor wafer as recited in claim 33, wherein the top electrode has a center region, a first surface and a second surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the second surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface of the top electrode which is located over the surface of the semiconductor wafer.

37. A method for high aspect ratio semiconductor etching, comprising:

providing a plasma etch processing chamber, the plasma etch processing chamber including a top electrode, a wafer support chuck, and a pair of RF power supplies, and the plasma etch processing chamber being configured in an operational state;

striking a plasma in a plasma region of the plasma etch processing chamber, the plasma region being defined between an electrode surface of the top electrode and a wafer surface of a wafer positioned on the wafer support chuck;

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode, the first surface of the plasma sheath being proximate to the top electrode; and

increasing a bias voltage over the wafer surface while decreasing the bias voltage over the electrode surface of the top electrode and without increasing a plasma density.

38. The method for high aspect ratio semiconductor etching of claim 37, further comprising increasing an ion bombardment energy on the wafer surface.

39. The method for high aspect ratio semiconductor etching of claim 37, wherein the top electrode has a center region, a first surface and the electrode surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the electrode surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the electrode surface of the top electrode which is located over the wafer surface.

40. The method for high aspect ratio semiconductor etching of claim 37, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of a second surface of the plasma sheath, the second surface of the plasma sheath being defined proximate to the wafer surface.

APPENDIX B

EVIDENCE APPENDIX

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/611,037
Applicant:	:	Kuthi, et al.
Filed:	:	July 6, 2000
Title:	:	METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE
TC/A.U.	:	1763
Examiner	:	Alejandro Mulero, L.
Atty. Docket No.	:	LAM1P077A

Declaration Under 37 CFR §1.132

I, Lumin Li, declare as follows:

1. I am a named inventor in the subject application. I earned an undergraduate degree in Electronic Engineering from Southeast University, and Ph.D. degree in Electrical Engineering from Colorado State University. I currently work in reactor design and process applications of plasma etcher, and have been employed for 11 years. For the past 8 years, I have been with Lam Research Corporation working on new dielectric etcher development.

2. I have reviewed the patent to Tomita et al. (U.S. Patent No. 5,593,540), the reference patent. The reference patent teaches how to prevent polymer deposition in the small holes of a showerhead electrode by high speed of gas flow. To achieve a mass flow speed of at least 620 $kg/m^2/hr$, the reference specifies the diameter of the holes in the showerhead must be smaller than 0.6 mm. The reference specifies 0.6 mm as the maximum diameter of the hole. Any hole larger than 0.6 mm will reduce gas speed and cannot prevent polymer deposition.

3. Our claimed invention described in the subject application is in the field of plasma physics. Our claimed invention teaches how to reduce sheath voltage next to the top electrode. By forming the plasma sheath inside the holes, the surface area of the plasma sheath next to the top electrode is increased, and its potential is reduced. The holes in the claimed invention must big enough to allow plasma to exist inside to form a hollow cathode discharge.

4. The diameter of the holes on the electrode showerhead is very critical for showerhead design. Increasing gas flow speed, and increasing the surface area of a plasma sheath are in different fields and have different technological focus. A large diameter of hole will reduce backside pressure, and will reduce gas flow speed through the holes. As a result, polymer may deposit inside holes. The reference patent specifies the maximum diameter of hole. Any hole larger than 0.6 mm will reduce gas speed and cannot prevent polymer deposition. On the contrary, hole size in our claimed invention must be bigger than a thickness of the plasma sheath to allow the sheath to form inside the hole. We specified the minimum hole size of 0.5 mm. The diameter of any hole larger than 0.5 mm will meet the requirement for a hole size, depending on various process parameters, including plasma sheath thickness.

5. Plasma sheath thickness depends on pressure, power and chemistry. For different etch applications, pressure in our etcher could vary from 10 mT to 2T, power could be 50W to 6KW, and there are more than 16 available gases. In order to include a wide range of plasma etch process regimes, we chose a diameter of 0.5 mm conservatively as the minimum size for the worst case with a high pressure, low power, and heavy polymer contents. For most of our applications, we prefer diameter of showerhead holes to be 2 ~ 10 mm.

6. Diameter of showerhead holes must be very small not only for gas flow speed, but also for preventing plasma light-up inside the hole. It is well known that when the hole is too large, and at high pressure, according to Paschen curve, plasma will ignite inside the hole. When plasma exists inside the hole, dense plasma inside of the hole will dissociate more species and generate more polymers inside the holes. As a result, there is or will be more polymer deposition. When plasma lights-up inside a hole, a sheath with high potential will accelerate ions and sputter away the electrode material. Plasma ignited inside a hole of showerhead is not desirable for a plasma etcher. The fast erosion of the electrode will quickly affect process repeatability, increase polymer deposition, and reduce lifetime of showerhead. It is a basic rule in plasma etcher design that the showerhead should prevent plasma light-up inside the hole. Our claimed invention purposely increases hole size and forms plasma in a portion of the hole, and is a

special case in which an increase in ion's energy on the wafer is critical for certain etch applications.

7. In our claimed invention, there are two different diameters of each hole specified for electrode showerhead design. The diameter of the hole in the top end and close to gas source (the gas feed holes) is 0.1 mm which is designed to prevent plasma from entering the holes and light-up inside of the holes and on a backside of the shower head. The diameter of the holes in the lower end and in contact with plasma (the electrode openings) is 0.5 mm which is designed to create plasma inside hole, increase the surface area of the plasma sheath next to the top electrode and increase the potential at the opposite electrode.

8. The objective of the reference patent is preventing polymer deposition. The size of the holes in the showerhead must be small enough to obtain the certain disclosed flow speed. At the same time, the flow speed must be maintained to prevent plasma light up inside the holes. A diameter of 0.6mm does not inherently shift the plasma sheath into the openings and create a surface area next to the electrode that is larger than the surface area that is next to the wafer. It is against common sense, basic plasma physics, and design rules for those skilled in the art -- that is, one of average competence and expertise in the field of plasma etch, would not modify the reference in such a manner as to increase size of the holes and purposely create plasma inside holes.

9. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC §1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

LUMIN LI

9-3-03
DATE